

What is claimed:

1 1. A semiconductor device comprising:
 2 a protective insulation layer;
 3 a pad opening section provided in the protective insulation layer;
 4 a wiring layer which the pad opening section reaches; and
 5 a wiring layer provided at a level lower than the wiring layer which the pad opening
 6 section reaches,
 7 wherein the wiring layer provided at a level lower than the wiring layer which the
 8 pad opening section reaches is formed outside a region of the pad opening section as viewed
 9 in a plan view.

1 2. A semiconductor device according to claim 1, wherein the wiring layer which
 2 the pad opening section reaches is composed of one layer.

1 3. A semiconductor device according to claim 1, wherein the wiring layer which
 2 the pad opening section reaches is composed of two layers.

1 4. A semiconductor device according to claim 1, wherein the wiring layer which
 2 the pad opening section reaches has a thickness that is greater than that of the wiring layer
 3 provided at a level lower than the wiring layer which the pad opening section reaches.

1 5. A semiconductor device comprising:
 2 a first wiring layer formed above a semiconductor layer through a first interlayer
 3 insulation layer;
 4 a second wiring layer that provides a pad section formed above the first wiring layer
 5 through a second interlayer insulation layer;
 6 a protective insulation layer formed above the second wiring layer and the second
 7 interlayer insulation layer; and
 8 a pad opening section provided in the protective insulation layer,

9 wherein an upper surface of the first interlayer insulation layer includes a first region
10 where the protective insulation layer is formed vertically thereabove, and
11 the first wiring layer is formed on the first region.

1 6. A semiconductor device according to claim 5, wherein
2 the upper surface of the first interlayer insulation layer further comprises a second
3 region where the pad opening section is formed vertically thereabove, and at least part of the
4 second interlayer insulation layer is formed on the second region.

1 7. A semiconductor device according to claim 5, wherein the first wiring layer
2 includes a plurality of wiring layers in the same layer, and the plurality of wiring layers are
3 formed on the first region.

1 8. A method for manufacturing a semiconductor device, the method comprising
2 the steps of:

- 3 (a) forming a wiring layer on an interlayer insulation layer;
4 (b) forming a protective insulation layer on the interlayer insulation layer and the
5 wiring layer; and
6 (c) forming a pad opening section in the protective insulation layer, which reaches
7 the wiring layer,

8 wherein the semiconductor device includes a wiring layer provided at a level lower
9 than the wiring layer to which the pad opening section reaches,

10 wherein the pad opening section is formed such that the wiring layer provided at a
11 level lower than the wiring layer to which the pad opening section reaches is formed outside
12 a region of the pad opening section as viewed in a plan view.

1 9. A method for manufacturing a semiconductor device according to claim 8,
2 wherein the wiring layer which the pad opening section reaches is composed of one layer.

1 10. A method for manufacturing a semiconductor device according to claim 8,
2 wherein the wiring layer which the pad opening section reaches is composed of two layers.

1 11. A method for manufacturing a semiconductor device according to claim 8,
2 wherein the wiring layer which the pad opening section reaches has a thickness that is
3 greater than that of the wiring layer provided at a level lower than the wiring layer which the
4 pad opening section reaches.

1 12. A semiconductor device according to claim 5, wherein the first wiring layer
2 is only formed on the first region.

1 13. A semiconductor device according to claim 6, wherein the first wiring layer
2 is only formed on the first region and the second interlayer insulating layer is formed over
3 the entire second region.

1 14. A semiconductor device as in claim 13, wherein a portion of the second
2 interlayer insulating layer is formed over the first region.

1 15. A semiconductor device as in claim 5, further comprising:
2 a third wiring layer positioned between the first wiring layer and the second wiring
3 layer; and
4 a third interlayer insulation layer positioned between the first interlayer insulation
5 layer and the second interlayer insulation layer.

1 16. A semiconductor device as in claim 15, wherein the third wiring layer is
2 connected to the first wiring layer through a plurality of first plugs and the third wiring layer
3 is connected to the second wiring layer through a plurality of second plugs, and the first
4 plugs and the second plugs are positioned to be offset from each other in a vertical direction.

1 17. A method for manufacturing a semiconductor device, comprising:
2 forming a lower level wiring layer;
3 forming an lower level interlayer dielectric layer on and adjacent to the lower level
4 wiring layer;
5 forming an upper level wiring layer above the lower level interlayer dielectric layer,
6 wherein the lower level wiring layer is electrically connected to the upper level wiring layer;
7 forming a protective insulation layer on the upper level wiring layer;
8 removing a first portion of the protective insulation layer over the upper level wiring
9 layer and over the lower level interlayer dielectric layer to form a pad opening section of the
10 upper level wiring layer,
11 wherein a second portion of the protective insulation layer located vertically above
12 the lower level wiring layer remains after removing the first portion of the protective layer;
13 and
14 wherein no portion of the lower level wiring layer is disposed vertically below the
15 pad opening section.

1 18. A method as in claim 17, further comprising forming an intermediate wiring
2 layer and an intermediate interlayer dielectric layer; wherein the intermediate wiring layer is
3 positioned above the lower level wiring layer and below the upper level wiring layer; and
4 the intermediate interlayer dielectric layer is positioned above the lower level interlayer
5 dielectric layer and below the upper level wiring layer.

1 19. A method as in claim 18, wherein no portion of the intermediate lower level
2 wiring layer is disposed vertically below the pad opening section.

1 20. A method as in claim 18, further comprising:
2 forming the lower level wiring layer to be electrically connected to the intermediate
3 level wiring layer;
4 forming the intermediate level wiring layer to be electrically connected to the upper
5 level wiring layer;
6 forming the lower level wiring layer to include has a thickness that is less than that
7 of the lower level interlayer dielectric layer;
8 forming the intermediate level wiring layer to include a thickness that is less than
9 that of the intermediate level interlayer dielectric layer;
10 forming a plurality of lower level plugs to electrically connect the lower level wiring
11 layer to the intermediate level wiring layer;
12 forming a plurality of intermediate level plugs to electrically connect the
13 intermediate level wiring layer to the upper level wiring layer; and
14 wherein the intermediate plugs are formed to be offset from the lower level
15 intermediate plugs in a vertical direction.

1 21. A method as in claim 17, further comprising forming a reflection prevention
2 film on the upper level wiring layer.

1 22. A method as in claim 21, further comprising removing the reflection
2 prevention film from the pad opening section of the upper level wiring layer.

1 23. A device as in claim 5, further comprising a reflection prevention film
2 formed on the second wiring layer.